Notice of Allowability	Application No.	Applicant(s)	
	10/840,018	DOI ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/6/04*.

2. ☒ The allowed claim(s) is/are *1-10*.

3. ☒ The drawings filed on *06 May 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 5/6/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

The present invention relates to a test apparatus which tests the quality of an electronic device where the internal clock of the device has a jitter. The claimed invention (claim 1 as the only independent claim) recites the novel combination of the following features:

A test apparatus for testing an electronic device, comprising: a reference clock generating unit for generating a reference clock;

a pattern generating unit for generating a test pattern synchronously with said reference clock to test said electronic device;

a waveform formatting unit for receiving said test pattern and inputting a formatted pattern which results from formatting said test pattern to said electronic device;

a first timing generator for generating a timing signal;

an output signal sampling circuit for sampling an output signal outputted by said electronic device in response to said test pattern at timing based on said timing signal generated by said first timing generator;

and a judging unit for judging quality of said electronic device based on a sampling result of said output signal sampling circuit,

wherein said first timing generator comprises:

a first variable delay circuit unit for receiving, delaying and outputting said reference clock;

and a first delay control unit for controlling a delay amount of said first variable delay circuit unit,

and said first delay control unit comprises:

a first basic timing data setting unit to which a first basic timing data is set in advance;

a first multi-strobe resolution data setting unit to which a first multi-strobe

resolution data is set in advance;

a first multi-strobe data calculating unit for calculating a first multi-strobe data based on said first multi-strobe resolution data in response to said reference clock;

and a first variable delay amount calculating unit for calculating said delay amount, by which said reference clock is to be delayed in said first variable delay circuit unit, based on said first basic timing data and first multi-strobe data.

The prior arts of record (Le et al. U.S. Patent No. 6,377,065 as an example of such prior arts) teaches a semiconductor test system that has a glitch detection function for detecting glitches in an output signal from a device under test to accurately evaluate a device under test (DUT), and pin electronics for transmitting the test pattern from the event generator to the DUT and receiving an output signal of the DUT and sampling the output signal by timings of the strobe signals, a pattern comparator for comparing sampled output data with the expected patterns, and a glitch detection unit for receiving the output signal from the DUT and detecting a glitch in the output signal by counting a number of edges in the output signal and comparing an expected number of edges.

The prior arts of record however fail to teach the above combination of claimed elements within a testing apparatus. As such, modification of the prior art of record can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the limitations set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination,

anticipate nor render obvious the claimed inventions. Hence, claims 1-10 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"A Dynamically Tracking Clock Distribution Chip with Skew Control" by Chengson et al. in 1990 Proceedings of the IEEE Custom Integrated Circuits Conference Publication Date: 13-16 May 1990 page(s): 15.6/1-15.6/4 NSPEC Accession Number: 3863856

This paper teaches a single-chip clock distribution circuit which is a self-calibrating synchronization system that receives a periodic, digital clock signal as a reference and generates multiple system clock signals that dynamically track and are synchronized to the reference clock across temperature, voltage, and process variations. This chip is used as an integral part of the clock distribution for a fault-tolerant computer system. Results from ATE and bench testing of this clock chip are presented. The edge rate, granularity, pin-to-pin skew, ASIC to non-ASIC delay line,

and clock jitter characteristics are verified to exceed collectively the specifications of commercially available products.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
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